Organic interposer, 2.5D structure like, development for MCM and Heterogeneous packaging

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Agenda

- Trend of SiP Package
- Introduction of Organic Interposer: i-THOP®
  “integrated Thin Film High Density Organic Package”
- Internal development status
- 2.5D structure like, i-THOP® 2.3D type
- Summary
Trend of SiP Package

- Stacked chip package
- Multi Chip module
- Package on Package
- 2.5D Silicon interposer
- FO-WLP tech.

Mostly chip first/middle solution

- Fine line interconnection between dice: L/S less than 5/5um
# Introduction of Organic Interposer

**Based on Trend of SiP Package...**

<table>
<thead>
<tr>
<th>Key item</th>
<th>Die first/middle solution</th>
<th>Advanced fine line formation</th>
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</thead>
<tbody>
<tr>
<td><strong>Issues or Concerns</strong></td>
<td>- KGD loss</td>
<td>- Difficult to achieve with current BU material and process</td>
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<td>- Tight requirements for material, considering issues with mold (e.g. Warpage)</td>
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<td>L/S: Less than 10/10um</td>
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Shinko would like to offer “Chip Last” solution, integrating such fine traces on conventional substrate materials.
i-THOP® (Integrated Thin Film High Density Organic Package)

- **i-THOP® Technology Introduction**
  - Thin film layer directly integrated conventional substrate
  - Shinko offers the i-THOP® Technology as a “Chip last solution”

**Ex. i-THOP® 2.1D type structure**

**Design specification in Fine wiring layers**
- Min. FC Pad Pitch = 40μm
- Min. L/S = 2/2μm
- Min. Via/Land Dia. = 10/21μm
- Metal Thickness = 2μm
- Insulation Thickness = 5μm

Conventional build-up substrate

- ✓ * max. metal layer count for thin film layer: 4 layers including Cu pads

“Design and detail dimensions are subject to change.”
Introduction of Organic Interposer: i-THOP®

**i-THOP® 2.1D type X-section view**

- **Cu pad (Top layer)**
  - Min. 40μm pitch
  - Φ25μm Cu pad
  - Φ10μm via

- **Top view: ENEPIG pad**

- **Photo via: Min. 10μm dia**

- **Min. L/S=2/2μm on the thin film resin**

- **Laser via & Photo via**
  - Φ10μm photo via
Internal Development Status

- **Trend of High-end Package substrate**
  - Package size becomes larger
  - Number of dice for integration are increased
  - Build-up layer counts are increased

**Current**

**Near Future**

- TAT for production: Long term
- Package yield: Decrease due to size effect
- Package cost: Increase mainly due to panel utilization
Shinko is now considering focusing on i-THOP® “2.3D type”.

### Comparison Table with current 2.1D type

<table>
<thead>
<tr>
<th></th>
<th>2.1D type</th>
<th>2.3D type</th>
<th>2.5D type</th>
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</thead>
<tbody>
<tr>
<td><strong>Structure</strong></td>
<td><img src="image1" alt="2.1D structure" /></td>
<td><img src="image2" alt="2.3D structure" /></td>
<td><img src="image3" alt="2.5D structure" /></td>
</tr>
<tr>
<td><strong>Pros</strong></td>
<td>No solder interconnect between interposer</td>
<td>KGS* and KGTFS** combination</td>
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</tr>
<tr>
<td></td>
<td>Better electrical performance</td>
<td>Larger size &amp; layers</td>
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<td></td>
<td>Simple supply chain management</td>
<td>Shorter manufacturing lead time</td>
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<td>Simple supply chain management</td>
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</tr>
<tr>
<td><strong>Cons</strong></td>
<td>Long lead time</td>
<td>Challenging interposer assembly</td>
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</tr>
<tr>
<td></td>
<td>Cost and Yield impact by size and layer count</td>
<td></td>
<td>Total assembly</td>
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<td></td>
<td></td>
<td></td>
<td>Possibility to increase total routing layers</td>
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</tbody>
</table>

KGS* = Known Good Substrate  
KGTFS** = Know Good Thin Film Substrate
2.5D structure like, i-THOP® 2.3D type

Structure of i-THOP® 2.3D type

Key technology
- Chemical mechanical polishing
- Seed layer sputtering
- Photo dielectric

Key technology
- Support carrier process
- Warpage control
- Assembly material and method

Joint portion
- SnBi solder
- NCF
- Cu post on BU substrate

Rigid layer

Thin film layer
= Multi die area size

Build-up substrate
i-THOP® 2.3D type

1st TV Demonstration

Thin i-THOP®

Size: 44 x 31 x 0.071mm
Stack up: 4+1

Substrate (DLL®)

Size: 65 x 65 x 1.73mm
Stack up: 5/2/5

Interposer assembly
i-THOP® 2.3D type

Ref. i-THOP® 2.1D type

Through TV demonstration
- Feasibility confirmation of SnBi solder joint with NCF
- Warpage trend check with 2 different core materials
- Feasibility confirmation of FC assembly on i-THOP® 2.3D type
**i-THOP® 2.3D type**

**Effectiveness of LTS (low temp. solder) on stress reduction**

**Analysis condition**
- Stress free temperature
  - Sn-Bi: 180deg.C
  - Sn-Ag-Cu: 240deg.C
- Analysis temperature: 25deg.C

**Strain at stack up portion**

- **Sn-Bi**
- **Sn-Ag-Cu**

**Die Area Warpage at Room Temp.**

- Sn-Bi: -13.2µm
- Sn-Ag-Cu: -22.1µm

**Strain at stack up portion**

- **Solder**
  - Sn-Bi: 0.0101 (90% reduction)
  - Sn-Ag-Cu: 0.1111

- **Copper pad**
  - Sn-Bi: 0.0131
  - Sn-Ag-Cu: 0.0848 (85% reduction)

**✓ SnBi solder gives us benefit of warpage and joint strain reduction.**
CTE of core layer: Material A > Material B

Warpage is strongly influenced by core material of lower substrate.

However, it is similar warpage variation on 2.3D type to 2.1D type in both cases.
Shinko would like to offer “Chip last” solution for a new SiP packaging.

i-THOP® is introduced, which has several structure type.

Shinko is now getting forces on i-THOP® 2.3D type even though 2.1D type development was advanced.

Current 2.3D type development status
- Process development and Internal TV demonstration stage
- Feasibility of SnBi solder joint with NCF is confirmed
- The Warpage data without die is similar to 2.1D type case.

Further development
- Feasibility confirmation of FC die bonding on i-THOP® 2.3D type
- Obtain reliability data w/ and w/o top dice (TCT, HTS, uHAST)
- 2nd TV demonstration, applying feedback from 1st one
Interconnecting our Future