中国系统级封装大会
SiP Conferences China 2017
2017年10月19 - 20日  深圳蛇口希尔顿南海酒店
扫一扫，关注大会动态
Advanced Packaging Materials and Technologies for Sophisticated SiPs
**What is Bakelite?**

Phenolic resin is synthesized by phenol and formalin.

1907  Dr. L.H Bäekeland invented in USA.

★The world first’s plastic is Phenolic resin.

Trade Name「Bakelite」

1911  Dr. Takamine got the license for domestic production.

Sankyo company (currently Daiichi-Sankyo Co., Ltd) started a trial production of phenol.

1955  Sumitomo Bakelite Co., Ltd was found.

**History**

L.H Bäekeland [1863~1944]

Dr. Takamine [1854~1922]

Encapsulation material for semiconductors

Molded products for automobiles

Medicine packaging
Increase data transfer amount
→ Increase I/O count
→ Fine L/S RDL technology to achieve high speed data transfer

No change I/O count
Accelerate modularization with component

Sophisticated SiPs coming...
SiPs: Several Technology Requirements

- EMI Shielding
- Sensitive Device Protection
- Shallow LASER Marking
- Solder Bump Protection
- Narrow Gap Filling
- High Thermal Conductivity
- Multi Layer Thinner Substrate
Sumitomo Bakelite “One Stop Solution”

Buffer coating / PID by
SUMIREXCEL CRC
WW No.1 share for buffer coating
High speed & High resolution

Wafer Dicing using
SUMILITE FSL
Special technology for ESD less film
Fine pattern formability

Interposer building by  λZ®
(Prepreg, Core and SR are available)
Low CTE, Low dimension change
High stiffness, R to R support.

Encapsulation by SUMIKON EME
WW No.1 share
Broad lineup to cover all PKG type
and molding method

Die bonding by
SUMIREXCEL CRM
WW No.2 share
broad lineup for various PKG

Die bonding by
SUMIREXCEL CRM
WW No.2 share
broad lineup for various PKG

Easy SMT process handling by
SUMILITE CSL
Special technology for
ESD less cover tape

Sumitomo Bakelite can support from Wafer to PKG
Contents

✓ Technology Development for SiP
  - Narrow Gap Filling
  - Solder Bump Protection
  - Warpage Control
  - Shallow LASER Marking
  - Fragile Component Protection
  - EMI Shielding
  - High Density Component Arrangement

✓ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
Contents

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✔ New Trend
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  - Low Df Material for 5G
Narrow Gap Filling

Filler in Molding Compound

Large filler stuck and cause incomplete filling.

→ Apply the filler with top cut
Narrow Gap Filling

◆ Test die with Cu pillar

- Die size: 10mm x 10mm
- Pillar pitch: 200um
- Pillar height: 5um
- Pillar diameter: 100um

Die bonding on substrate at 4 corners of Cu die

Molding

Take out from substrate

Observe filling performance

EMC

Substrate

Test die

5um

Good filling

Bad filling

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Narrow Gap Filling

5um gap filling

EMC with 12um sieved
Filling : NG

EMC with 5um sieved
Filling : OK

✓ Fine filler top cut is important for narrow gap filling
Newtonian fluid
Viscosity does not depend on the shear rate

Pseudoplastic fluid

Unbalanced flow

Newtonian fluid

Balanced flow
### Narrow Gap Filling

#### Newtonian fluid

Study of filler surface modification in EMC

<table>
<thead>
<tr>
<th>Grade</th>
<th>STD</th>
<th>Sample 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filler Treatment</td>
<td>non</td>
<td><strong>Surface Modification</strong></td>
</tr>
</tbody>
</table>

→ Filler with surface modification show Newtonian-fluid like behavior.

< Filling Test Result : FCCSP >

- Die size 10 x 10mm
- Bump height 35um x Pitch 150um

P-lapping to check void

✓ Sample will be ready soon.
Contents

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  - Low Df Material for 5G
Solder Bump Protection

Solder bump in SiP is larger than micro-bump in FCCSP.

→ Several factors need to be considered for protection from damage.

✓ Some examples of study are introduced as following pages.
Solder Bump Protection

Solder extrusion after reflow: Effect of Filler Size in EMC

- Random flash occurred by Grade B.
- Random flash was improved by Grade A.
- There are some void around bumps after mold.
- Moisture in void explodes and leads delamination and solder flash.
- Smaller Filler is better.

EMC Information

<table>
<thead>
<tr>
<th></th>
<th>Grade A</th>
<th>Grade B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sieving size</td>
<td>32um</td>
<td>20um</td>
</tr>
<tr>
<td>Ave filler size</td>
<td>10um</td>
<td>5um</td>
</tr>
</tbody>
</table>

After MSL & reflow x 3

- Micro void
- Solder Flash
Solder Bump Protection

Solder extrusion after reflow: Effect of Modulus at 260°C of EMC

EMC Information

<table>
<thead>
<tr>
<th></th>
<th>Grade C</th>
<th>Grade D</th>
<th>Grade E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resin Type</td>
<td>C</td>
<td>D</td>
<td>E</td>
</tr>
<tr>
<td>Modulus at 260°C</td>
<td>2000</td>
<td>1000</td>
<td>500</td>
</tr>
<tr>
<td>Flash area</td>
<td>100</td>
<td>30</td>
<td>0</td>
</tr>
</tbody>
</table>

Low Modulus (=stress) is important.

<Grade C after reflow>

<Grade E after reflow>

Solder bump (200um)

Solder Flash

No flash

✓ Low Modulus (=stress) is important.
Contents

✓ Technology Development for SiP
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✓ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
## Warpage Control

<table>
<thead>
<tr>
<th>Volume</th>
<th>EMC &lt; PCB</th>
<th>EMC &gt; PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>PKG structure</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>Warpage Direction</td>
<td><strong>RT</strong></td>
<td><strong>260degC</strong></td>
</tr>
<tr>
<td></td>
<td><img src="image3.png" alt="Image" /> cry shape</td>
<td><img src="image4.png" alt="Image" /> smile shape</td>
</tr>
<tr>
<td></td>
<td><strong>smile shape</strong></td>
<td><strong>cry shape</strong></td>
</tr>
<tr>
<td>EMC property direction</td>
<td><strong>High CTE / Modulus</strong></td>
<td><strong>Low CTE / Low Modulus</strong></td>
</tr>
</tbody>
</table>

- EMC with high / low CTE & Modulus is required to control warpage.
- For Ultra thin PCB, substrate with carrier is needed to avoid bending.
Warpage Control : EMC

EMC with high CTE

New filler can achieve high CTE

TMA

- Silica
- New filler

Phase transition

187 ppm

18 ppm

79 ppm

26 ppm

63 ppm

200

150

100

50

0

0

100

200

300

Temp. [degC]

TMA [um]

α phase (RT)

β phase (HT)

Ca. 230degC

phase transition (reversible)

Warpage Test by Thinner PKG

PKG Size

<table>
<thead>
<tr>
<th>PKG Size</th>
<th>mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size</td>
<td>14x14</td>
</tr>
<tr>
<td>Bump pitch</td>
<td>10x10x0.06</td>
</tr>
<tr>
<td>Bump Height</td>
<td>um</td>
</tr>
<tr>
<td>Mold Thickness</td>
<td>um</td>
</tr>
<tr>
<td>Subs. thickness*1</td>
<td>um</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>RT</th>
<th>HT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Warpage [um]</td>
<td>44</td>
<td>37</td>
</tr>
<tr>
<td></td>
<td>-132</td>
<td>-87</td>
</tr>
</tbody>
</table>

EMC w/ Silica

EMC w/ New filler

✓ Warpage is improved

*1) Substrate : Low CTE type
**Warpage Control : EMC**

**EMC with low CTE**

Negative CTE filler under development

<table>
<thead>
<tr>
<th>Grade</th>
<th>(Ref)</th>
<th>Leg 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filler type</td>
<td>-</td>
<td>silica</td>
</tr>
</tbody>
</table>

General Property

<table>
<thead>
<tr>
<th>Property</th>
<th>(Ref)</th>
<th>Leg 1 (+Negative)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spiral Flow</td>
<td>cm</td>
<td>&gt;260</td>
</tr>
<tr>
<td>Gel Time</td>
<td>sec</td>
<td>45</td>
</tr>
<tr>
<td>CTE1 / 2</td>
<td>ppm/°C</td>
<td>13 / 43</td>
</tr>
<tr>
<td>Tg</td>
<td>°C</td>
<td>145</td>
</tr>
<tr>
<td>F. Modulus (25°C)</td>
<td>MPa</td>
<td>19000</td>
</tr>
<tr>
<td>F. Modulus (260°C)</td>
<td>MPa</td>
<td>700</td>
</tr>
</tbody>
</table>

- Negative CTE filler can decrease CTE.
- But poor flowability due to flake shape.

→ Spherical shape under development.
Thinner substrate need carrier board to avoid bending. → **Temporary Bonding Film** for carrier is required.

Process Image of **photo sensitive Temporary Bonding Film (TBF)**

- **Carrier board**
- **Strip substrate**
- **Imaging** (Photo sensitive only unit area)
- **Attaching strip substrate**
- **Laminate**
- **Adhesion of photo sensitive area lowered**
- **Die mount**
- **Molding**
- **Substrate Bending**
  - 80umt
  - 50umt

**Warpage Control : Substrate**

**Temporary Bonding Film**
# Warpage Control (Thinner Substrate)

## Detaching ability (Subs)

<table>
<thead>
<tr>
<th>Process</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die mount (260 deg.C reflow)</td>
<td>Good (non-Delamination)</td>
</tr>
<tr>
<td>EMC Molding (175deg.C/5h)</td>
<td>Good (non-Delamination)</td>
</tr>
<tr>
<td>Detach</td>
<td>Good <strong>No Residue on Substrate Surface</strong></td>
</tr>
</tbody>
</table>

We have been developing film for matching this process.
Contents

✓ Technology Development for SiP
  - Narrow Gap Filling
  - Solder Bump Protection
  - Warpage Control
  - Shallow LASER Marking
  - Fragile Component Protection
  - EMI Shielding
  - High Density Component Arrangement

✓ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
Shallow depth after LASER marking

Thinner gap on tall component

**Shallow LASER Marking**

**Study of EMC**

<table>
<thead>
<tr>
<th>Property</th>
<th>STD</th>
<th>New Additive</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coloring agent</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Property</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spiral Flow</td>
<td>cm</td>
<td>135</td>
</tr>
<tr>
<td>Gel Time</td>
<td>sec</td>
<td>59</td>
</tr>
<tr>
<td>CTE1</td>
<td>ppm</td>
<td>11</td>
</tr>
<tr>
<td>CTE2</td>
<td>ppm</td>
<td>43</td>
</tr>
<tr>
<td>Tg</td>
<td>‘C</td>
<td>130</td>
</tr>
<tr>
<td>F. Modulus (25°C)</td>
<td>N/mm²</td>
<td>20000</td>
</tr>
<tr>
<td>F. Modulus (260°C)</td>
<td>N/mm²</td>
<td>500</td>
</tr>
<tr>
<td>Specific Gravity</td>
<td>-</td>
<td>1.98</td>
</tr>
<tr>
<td>Shrinkage</td>
<td>%</td>
<td>0.17</td>
</tr>
</tbody>
</table>

Note: The value on this table is typical one.

 ✓ EMC with new additive to achieve good visibility and lower depth.
# Shallow LASER Marking

## LASER Marking Depth and QR Cord Recognition Test

Laser-making Equipment: SFL263 (EO Technics), Wavelength: 1064nm, Max Power: 40W

<table>
<thead>
<tr>
<th>Marking Condition</th>
<th>270mm/s, 1.2A</th>
<th>400mm/s, 1.2A</th>
<th>300mm/s, 1.0A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EMC w/ STD</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>depth</td>
<td>25um</td>
<td>13um</td>
<td>8um</td>
</tr>
<tr>
<td><strong>QR recognition</strong></td>
<td>Hard</td>
<td>hard</td>
<td>hard</td>
</tr>
<tr>
<td><strong>EMC w/ New Additive</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>depth</td>
<td>20um</td>
<td>10um</td>
<td>5um</td>
</tr>
<tr>
<td><strong>QR recognition</strong></td>
<td>hard</td>
<td>hard</td>
<td>easy</td>
</tr>
<tr>
<td><strong>EMC w/ New Additive</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>* after sputter*</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>depth</td>
<td>20um</td>
<td>10um</td>
<td>5um</td>
</tr>
<tr>
<td><strong>QR recognition</strong></td>
<td>easy</td>
<td>easy</td>
<td>easy</td>
</tr>
</tbody>
</table>

*hard / easy*: recognition test by phone camera (10pcs).
“hard” needs to raise the contrast by light.

✔ New Additive achieve shallow depth (5um) and good recognition due to higher contrast.
Contents

✓ Technology Development for SiP
  - Narrow Gap Filling
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  - High Density Component Arrangement

✓ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
Low pressure molding as technical challenge

- To mold sensitive device
- To avoid huge molding machine by large panel molding

SAW/BAW with hollow structure

Study of low pressure molding as following page.

Target pressure: 3 MPa
## Test Vehicle
- Mold thickness : 330umt
- Substrate size : 245x75x0.2mmt (2 block)

## Filling Test Result

<table>
<thead>
<tr>
<th>EMC Grade</th>
<th>Filler cut (um)</th>
<th>NGFP*1 (MPa)</th>
<th>Transfer Pressure (MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>A</td>
<td>20</td>
<td>2.0</td>
<td>NG</td>
</tr>
<tr>
<td>B</td>
<td>12</td>
<td>0.9</td>
<td>OK*</td>
</tr>
<tr>
<td>C</td>
<td>20</td>
<td>0.5</td>
<td>OK</td>
</tr>
<tr>
<td>D</td>
<td>24</td>
<td>0.2</td>
<td>OK*</td>
</tr>
</tbody>
</table>

* No molding test but estimated.  *1) Narrow Gap Flow Pressure at 0.5mmt

---

**Molding Information**

* Mold chase VCH
  - Machine : GTM-X VCH
  - Plunger type : Resin ring type (AYC dome)
  - Mold temp. : 175°C
  - Pre-heat : 0sec
  - Tr. Speed : 1.2mm/s
  - Vacuum : 1.1kpa

---

**Further study for better filling at low pressure molding on going !**

Filling test by FCCSP

---
Fragile Component Protection

**Test Vehicle**
- Mold thickness : 330umt
- Substrate size : 245x75x0.2mmt (2 block)
- Die size : 5mmx5mmx0.10mmt
- Solder Bump : height 100um x Pitch 200um
- EMC : Grade-B

**Filling Test Result (Void under F/C)**

Tr. Pressure : 2MPa  
Tr. Pressure : 1MPa

- No void
- Void

✓ Filling under F/C until 2MPa is OK.
Contents

✔ Technology Development for SiP
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✔ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
EMI Shielding

Adhesion Study of EMC-Metal: EMC formulation

We studied adhesion of sputtering metal to EMC.

We counted the number of delamination.

Adhesion can be improved by EMC. Additional study keep going.
EMI Shielding

Adhesion Study of EMC-Metal: **Surface Activation**

**Activation**

EMC Substrate → Activation → Cu plating → Cu pealing test

**Cu pealing Test**

Peel strength tool (N/cm)

![Peel strength tool](image)

Graph:

- Peeling strength (N/cm)
- without: 2.5 N/cm
- with Activation: 5 N/cm

✓ Surface Activation also can enhance adhesion.
Contents

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✓ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
# High Density Component Arrangement

## Narrow space for die attach material in SiP

![Diagram](image)

It is very close for each unit in SiP. → Control die attach material is key.

## Table: Die attach film (cDDF) vs Die attach paste

<table>
<thead>
<tr>
<th></th>
<th>Die attach film (cDDF)</th>
<th>Die attach paste</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fillet control</td>
<td>No fillet</td>
<td></td>
</tr>
<tr>
<td>BLT control</td>
<td>No die tilt</td>
<td></td>
</tr>
<tr>
<td>Resin bleed</td>
<td>No resin bleed</td>
<td></td>
</tr>
</tbody>
</table>

✓ cDDF is better than die attach paste for SiP.
High Density Component Arrangement

<Features of cDDF>
- High electric conductivity (4E-4Ω.cm)
- Good reliability for various metal surface
- Low outgas during curing (0.1%)

■ Process Performance

<table>
<thead>
<tr>
<th>Die size</th>
<th>Dicing</th>
<th>Pick Up</th>
</tr>
</thead>
<tbody>
<tr>
<td>1x1mm²</td>
<td>No residue after picking up</td>
<td>No die fly after dicing</td>
</tr>
<tr>
<td>5x5mm²</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Die thickness: 200um)

■ Reliability

Level 3 + R260x3 Pass

■ Bonding control

No fillet & bleed after die bonding
Contents

✓ Technology Development for SiP
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✓ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
Key property of EMC for WLP : Warpage Control

Example of very large warpage

Example of good (small) warpage

Stress Index of EMC (=CTE1 x E1*)

* E1: Flexural modulus @25degC

✔ Lower stress index EMC can achieve low wafer warpage.
<table>
<thead>
<tr>
<th></th>
<th>EMC-1</th>
<th>EMC-2</th>
<th>EMC-3</th>
<th>EMC-4</th>
<th>LMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC</td>
<td>wt%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>90</td>
<td>89</td>
<td>89</td>
<td>90</td>
<td>85</td>
</tr>
<tr>
<td>CTE1</td>
<td>ppm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>E1</td>
<td>GPa</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>27</td>
<td>20</td>
<td>20</td>
<td>15</td>
<td>25</td>
</tr>
<tr>
<td>Stress index</td>
<td>189</td>
<td>180</td>
<td>160</td>
<td><strong>105</strong></td>
<td>250</td>
</tr>
</tbody>
</table>

**12” wafer warpage**

![Graph showing warpage](image)

**Unit coplanarity**

![Graph showing coplanarity](image)

- Lower stress index EMC also show low unit warpage.
**FOWLP SiP**

**Warpage Study of EMC-RDL**

- **Mold thickness:** 450umt
- **Die size:** 10.5mm □, 350umt
- **RDL:** CRC-8903, 1~4 layer (1layer=7umt)

### Table: CRC-8903 Properties

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>unit</th>
<th>Curing condition (degC x min)</th>
<th>EMC-8903</th>
</tr>
</thead>
<tbody>
<tr>
<td>Curing condition</td>
<td>10degC/ min</td>
<td>ppm/k</td>
<td>200 x 90</td>
<td>259</td>
</tr>
<tr>
<td>To</td>
<td>250</td>
<td>CTE</td>
<td>283</td>
<td>39</td>
</tr>
<tr>
<td>CTE</td>
<td>40~150degC</td>
<td></td>
<td>41</td>
<td>39</td>
</tr>
<tr>
<td>5% weight loss Temp.</td>
<td>3degC/ min</td>
<td></td>
<td>369</td>
<td>410</td>
</tr>
<tr>
<td>Tensile elongation</td>
<td>RT</td>
<td>(%)</td>
<td>52</td>
<td>55</td>
</tr>
<tr>
<td>Tensile modulus</td>
<td>RT</td>
<td>(GPa)</td>
<td>2.8</td>
<td>2.9</td>
</tr>
<tr>
<td>Tensile strength</td>
<td>RT</td>
<td>(MPa)</td>
<td>119</td>
<td>124</td>
</tr>
<tr>
<td>Water absorption</td>
<td>24hrs/ RT</td>
<td>(%)</td>
<td>1.5</td>
<td>1.4</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>1MHz/ RT</td>
<td></td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>Volume Resistivity</td>
<td>RT</td>
<td>ohm-cm</td>
<td>&gt;1.0E16</td>
<td>&gt;1.0E16</td>
</tr>
<tr>
<td>Surface Resistivity</td>
<td>RT</td>
<td>ohm</td>
<td>&gt;1.0E16</td>
<td>&gt;1.0E16</td>
</tr>
<tr>
<td>Dielectric Strength</td>
<td>RT</td>
<td>kV/mm</td>
<td>321</td>
<td>350</td>
</tr>
</tbody>
</table>

**Graph:**

- RDL layer number impact on warpage due to high CTE of RDL.
  - FC84% (SI=232)
  - FC90% (SI=40)

**Summary:**

- ✓ Considering EMC / RDL / PKG design is important.
Contents

✓ Technology Development for SiP
  - Narrow Gap Filling
  - Solder Bump Protection
  - Warpage Control
  - Shallow LASER Marking
  - Fragile Component Protection
  - EMI Shielding
  - High Density Component Arrangement

✓ New Trend
  - FOWLP SiP
  - Low Df Material for 5G
Utilization of milli-wave bands is increasing for high speed and large data transfer.

→ Low Df material at high frequency bands is required.
Low Df Material for 5G

Substrate Material

<table>
<thead>
<tr>
<th>Item</th>
<th>Unit</th>
<th>LAZ-6785KS-H</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass Cloth</td>
<td>Style</td>
<td>#1027</td>
</tr>
<tr>
<td>Df</td>
<td>10GHz</td>
<td>0.004</td>
</tr>
<tr>
<td>Dk</td>
<td>10GHz</td>
<td>3.6</td>
</tr>
<tr>
<td>RC</td>
<td>%</td>
<td>71</td>
</tr>
<tr>
<td>Tg</td>
<td>DMA</td>
<td>235</td>
</tr>
<tr>
<td>CTE (XY)</td>
<td>a1</td>
<td>12</td>
</tr>
<tr>
<td>Tensile Modulus</td>
<td>25C</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>260C</td>
<td>9</td>
</tr>
</tbody>
</table>

<Process-ability of Laser BVH drill process>

<table>
<thead>
<tr>
<th>ME</th>
<th><a href="mailto:5min.@80deg.C">5min.@80deg.C</a></th>
<th><a href="mailto:10min.@80deg.C">10min.@80deg.C</a></th>
</tr>
</thead>
<tbody>
<tr>
<td>LAZ-6785KS-H #1027_35um</td>
<td>No smear</td>
<td>No smear</td>
</tr>
</tbody>
</table>

*SW : 5min.@60deg.C, RE : 5min.@40deg.C

✓ Substrate with low Df is ready.
Low Df Material for 5G

Substrate Material : EMC

<table>
<thead>
<tr>
<th>Grade</th>
<th>Ref</th>
<th>New EMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resin Type</td>
<td>Standard</td>
<td>Low Df Type</td>
</tr>
<tr>
<td>General property</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Df @ 60GHz</td>
<td>0.009</td>
<td>0.004</td>
</tr>
<tr>
<td>Dk @ 60GHz</td>
<td>3.8</td>
<td>3.7</td>
</tr>
<tr>
<td>Spiral Flow</td>
<td>cm</td>
<td>195</td>
</tr>
<tr>
<td>Gel Time</td>
<td>sec</td>
<td>50</td>
</tr>
<tr>
<td>Alpha 1 / 2</td>
<td>x10^-5/degC</td>
<td>1.0 / 4.0</td>
</tr>
<tr>
<td>Tg</td>
<td>degC</td>
<td>150</td>
</tr>
<tr>
<td>F. Strength</td>
<td>@RT N/mm²</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td>@260 N/mm²</td>
<td>15</td>
</tr>
<tr>
<td>F. Modulus</td>
<td>@RT N/mm²</td>
<td>22000</td>
</tr>
<tr>
<td></td>
<td>@260 N/mm²</td>
<td>600</td>
</tr>
<tr>
<td>Water absorption</td>
<td>%</td>
<td>0.20</td>
</tr>
<tr>
<td>Mold shrinkage</td>
<td>%</td>
<td>0.12</td>
</tr>
</tbody>
</table>

Note: These values are not guaranteed, just typical one.

✓ EMC sample with Low Df is ready.
Summary

We keep exploring new material & technology to achieve your innovative product.
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